Design and Development of an FPGA Board for Software-Defined Radio Research

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Abstract: This paper describes the design and development of a cost-affordable yet powerful software-defined radio system. The main application environment of the board is in academia where it is used to deliver a multidisciplinary approach in a number of fundamental engineering topics in communications. A moderately fast ADC together with an audio DAC are used for the analog components while an off-the-shelf FPGA is used as the digital processing element. To demonstrate the board’s capabilities, hardware blocks to demodulate amplitude modulation and digital modulation were developed.

Keywords: software-defined radio; circuit design; FPGA; digital signal processing; analog demodulation

Introduction

Software-defined radio (SDR) has become the standard for communication receivers. Ever since the principle of software radio has been defined by Mitola (Mitola III 2000), this concept has been increasingly used. As such, it is important that it forms part of the undergraduate communications curriculum. With the development of more affordable components and systems, the design and implementation of software receivers has become widely available. Solutions can range from complete off-the-shelf receivers, such as the popular RTL-SDR dongle (RTL-SDR, no date; Wickert and Lovejoy 2015), to complete wide bandwidth systems (Ettus Research, no date). The advantage of these systems is that they help the novice user get started but provide little information on the underlying principles and subsequent implementation. A review has been carried by Xu et al. (2018). However, for those who want to implement from the ground up, digital technology has advanced to the point that this is possible. Using FPGA’s and interfacing boards, a complete SDR system can be designed and implemented (Digilent – Start Smart, Build Brilliant, no date; Terasic Inc. - Expertise in FPGA/ASIC Design, no date). Such a solution would be advantageous to the student as it is possible to have a multi-disciplinary approach which is both affordable and attainable. To date, no such platform with these requirements has been developed. However, designing an SDR system poses its own set of unique challenges to the student. The student has a challenging task in integrating different disciplines together in a single project. This is because subjects are delivered independently from each other without exposing the links between them. However, many real world projects are interdisciplinary in nature and require in-depth knowledge of various subjects. The need arises for the student to gain experience in interdisciplinary projects to see how different techniques integrate together. The aim of this paper is to demonstrate the design of a software-designed radio system made up of an ADC, DAC, and an FPGA. The demodulation of amplitude modulation and frequency modulation will be demonstrated. Though the design of such a system
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Background Information

may appear simple given the more advanced modulation schemes available, it requires knowledge from the field of communications, signals, analog and digital electronics, and digital design.

The rest of the paper is organized as follows: a literature review section will outline the key principles of software-defined radio together with the background theory of IQ Amplitude Demodulation and Frequency Demodulation. The implementation section will show how an SDR platform may be constructed using affordable ADCs, DACs, and FPGA. The results section will discuss the quality of results obtained. At the end of the paper, suggestions for future work are given.

Background Information

Literature Review

Figure 1: Software-defined radio system

Figure 1 shows a typical SDR system. The design of software-defined radio architectures has evolved over the years. In the beginning, SDR systems were made up of an antenna, a Loew noise amplifier (LNA), and a mixer to down-convert the signal to an intermediate frequency (IF) stage. After this process, the signal was digitized and processed. Processing may be done using either digital signal processing (DSP), field programmable gate array (FPGA), or general purpose processors (GPP). Recent systems have dispensed with the IF stage and the signal is sampled directly from the LNA stage as shown in Figure 2. This advance has been possible with the advent of high-speed analog-to-digital convertors and fast FPGA fabric. Another option is to use a USB dongle as an RF frontend and software running on a relatively modern computer. Furthermore, FPGAs with integrated RF-ADC’s (Zynq UltraScale+ RFSoC, no date) are able to digitize and process the signals on a single chip. An SDR system may have other modules to manage power or a user interface. Undergraduate students reading on the subject for the first time may find the subject too complex and this might put them off. However, with the availability of powerful yet affordable FPGAs and mid-range ADCs, a software-defined radio system may be built which delivers good performance, is expandable, and provides good didactic fundamentals.
**Background Theory**

*Amplitude Modulation*

A double sideband large carrier (DSB-LC) modulated signal follows the form as in the equation (1):

\[ v_{AM}(t) = \cos(2\pi f_c t) + \frac{m}{2} \cos(2\pi (f_c - f_m) t) + \frac{m}{2} \cos(2\pi (f_c + f_m) t) \]  

(1)

The depth of modulation is controlled by the modulation index \( m \). An index greater than 1 indicates that over-modulation is present and leads to a phase reversal of the signal and should be avoided. The DSB-LC signal may be demodulated either by using a non-coherent detector, such as a diode or coherent detection. A coherent method using a synchronous detector is preferred. A synchronous detector, as shown in Figure 3, uses a mixer to down-convert the modulated signal to baseband. The signal was passed through a low pass filter to recover the demodulate signal.

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**Figure 2:** SDR system using wideband A/D and D/A convertors

**Figure 3:** Local oscillator
One disadvantage of this method is that the phase of the carrier and the phase of the local oscillator (LO) do not match. Equation 2 shows the effects of a phase mismatch between the carrier and the LO.

\[ v_r = \cos(2\pi f_c t + \phi) \]  \hspace{1cm} (2)

\[ v_m = v_{AM} v_r \text{ and } f_c = f_r \]  \hspace{1cm} (3)

\[ v_m = \left[ \cos(2\pi f_c t) + \frac{m}{2} \cos(2\pi (f_c - f_m) t) + \frac{m}{2} \cos(2\pi (f_c + f_m) t) \right] \cos(2\pi f_c t + \phi) \]  \hspace{1cm} (4)

Expanding (4)

\[ v_m = \cos(4\pi f_c t) + \cos(\phi) + \frac{m}{4} \cos(2\pi (2f_c - f_m + \phi) t) + \frac{m}{4} \cos(2\pi (f_m + \phi) t) \]  \hspace{1cm} (5)

Removing frequency components at \( 2f_c \) leaves the baseband components:

\[ v_m = \cos(\phi) + \frac{m}{4} \cos(2\pi (f_m + \phi) t) + \frac{m}{4} \cos(2\pi (f_m + \phi) t) \]  \hspace{1cm} (6)

Simplifying (6) yields:

\[ v_m = \cos(\phi) + \frac{m}{2} \cos(2\pi f_m t) \cos(\phi) \]  \hspace{1cm} (7)

Equation 7 has a d.c. term and the original modulating frequency multiplied by the phase difference between the carrier and the local oscillator. When the phase difference \( \phi \) is \( 90^\circ \), the received signal goes to 0, hence an improved demodulation method which ignores the phase mismatch between the carrier and local oscillator was needed. This is the IQ demodulation method as shown in Figure 4.
Figure 4: Quadrature demodulation

The modulated signal is multiplied by the in-phase and quadrature components of the local oscillator. The signals are then bandpass filtered so only the baseband signals are retained and any dc. component is removed. The amplitude of the recovered signal is found out by taking the magnitude of the in phase and quadrature signals, hence any phase shifts between the carrier of the modulated signal and the locally generated carrier affect the signal amplitude. Equations 8 to 10 show the process.

For the in phase path after the band pass filter:

$$v_i = \frac{m}{2} \cos(2\pi f_m t) \cos(\phi)$$  \hspace{1cm} (8)

For the quadrature path after the bandpass filter:

$$v_q = \frac{m}{2} \cos(2\pi f_m t) \sin(\phi)$$  \hspace{1cm} (9)

After taking the magnitude operation, the resultant signal is the original message signal independent of any phase mismatch in the system:

**Frequency Modulation**

In frequency modulation, the frequency of the carrier is modulated by the signal. The depth of modulation is known as $\beta$, defined as the ratio of the change in the carrier frequency to the carrier frequency as in equation:

$$\beta = \frac{\Delta f}{f_m}$$  \hspace{1cm} (11)
Narrowband FM has a \( \beta \leq 0.316 \) in order to produce linear modulation. Wideband FM has a \( \beta > 0.316 \) and is non-linear in nature. Only a wideband FM modulation was considered, as the main interest was to demodulate commercial FM signals. An FM signal is generated by eq. (12):

\[
v_{FM} = A \cos(2\pi f_c t + \beta \sin(2\pi f_m t))
\]  

(12)

An FM signal may be demodulated using direct analog methods, mainly the Foster-Seeley (Helm and Grimes 1970) and ratio detectors. These techniques are purely analog and not used any more. Another option is to use an indirect method, the phase locked loop (PLL) (Zhihong, Zongqi, and Danjiang 2008). Advances in circuit design have made this technique the standard method for demodulating an FM signal. A block diagram of the PLL is shown in Figure 5.

![Phase locked loop block diagram](image)

**Figure 5: Phase locked loop**

The PLL is made up of 3 sections: (a.) the phase detector which finds the difference in phase between the incoming signal and the reference signal; (b.) a loop filter acts as a low pass filter to smoothen the varying phase difference; (c.) the voltage controlled oscillator (VCO) which changes the reference frequency in response to a d.c. voltage produced by the loop filter; and (d.) a low pass filter to remove the higher frequency components of noise. A locked PLL will have zero phase error and a steady phase difference between the input and reference frequency. Eq 16 gives the transfer function of the PLL.

\[
v_q = K_d (\theta_i - \theta_o)
\]  

(13)

Where \( v_d \) is the error voltage, \( \theta_i \) is the input phase and \( \theta_o \) is the output phase from the VCO, and \( K_d \) is the gain of the phase detector.

\[
V_c(s) = F(s) v_d(s)
\]  

(14)

Where \( F(s) \) is the transfer function of the loop filter:

\[
\theta_o(s) = \frac{K_d V_c(s)}{s}
\]  

(15)

Where \( K_o \) is the VCO gain.
The closed loop transfer function is obtained by combining equations to, which yields:

\[ H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d K_o F(s)}{s + K_d K_o F(s)} \]  \hspace{1cm} (16)

The control voltage to the VCO contains the original modulating signal after passing through the loop filter and divided by the gain factor of the VCO. Hence, in this case, the output of the loop filter serves as the output signal of the PLL. The design of the PLL is such that for a low distortion operation and the ability to track the incoming signal, the bandwidth of the PLL needs to be larger than the bandwidth occupied by the modulated signal. The transfer function of the PLL when in this mode is given by equation.

\[ \frac{V_c(s)}{w_i(s)} = \frac{1}{K_o} H(s) \]  \hspace{1cm} (17)

The PLL was implemented in an FPGA, hence the transfer function was re-written in the z domain as shown in equation.

\[ H(z) = \frac{K_d F(z) N(z)}{1 + K_d F(z) N(z)} \]  \hspace{1cm} (18)

Where \( F(z) \) is the transfer function of the loop filter and \( N(z) \) is the transfer of the NCO represented by

\[ N(z) = \frac{K_o z^{-1}}{1 - z^{-1}} \]

The transfer function for FM demodulation is given by equation:

\[ \frac{V_c(z)}{w_i(z)} = \frac{1}{K_o} H(z) \]  \hspace{1cm} (19)

Figure 6 shows the block diagram of the DPLL. The PLL is 2\(^{nd}\) order and type 2.

**Figure 6: z-transform representation of the phase locked loop**
Implementation

The signal processing outlined in the sections above was implemented using an FPGA. The system was split into three parts. The first part was the design of a data acquisition system to capture modulated data using an ADC. The second part consisted of hardware blocks to implement the demodulation techniques. Each of the demodulation techniques were implemented separately. The third part was an audio DAC to output the demodulated audio signal. Figure 7 shows the block diagram of the system.

![Figure 7: ADC and DAC sub systems](image)

A 12-bit Analog to Digital Convertor (AD9235-40) was chosen (AD9235 Datasheet and Product Info | Analog Devices, no date). The selected ADC has a sampling rate of 40Msps per second and an analog input bandwidth of 500MHz. A large bandwidth ADC was selected to accommodate future expansion and even the possibility of direct sampling from an antenna. The selected DAC was the 10 bit AD5333 (AD5333 Datasheet and Product Info | Analog Devices, no date). Both data convertors work with a single supply voltage of 5V, hence requiring no external power supply. A sampling frequency of 400kHz was selected which could accommodate the bandwidth of a commercial FM signal. The ADC was driven by a single ended-to-differential convertor for optimum performance. Both the antialiasing filter and the reconstruction filter were constructed on separate boards so the same hardware setup could be reused again.

A reference voltage of 1V was selected. This voltage was generated from the AD9235 buffered and supplied to the DAC. The incoming signal was offset by $V_{ref}/2$ to centre the signal to the mid-range of the ADC. An anti-alias filter with a cutoff frequency ($f_c$) of 200kHz preceded the ADC. After sampling, this offset was removed to use an internal 2's complement signed representation.

Mixing, for both AM and FM demodulation, was implemented in the digital domain by using a numerically controlled oscillator (NCO). An NCO uses an accumulator and a look-up table (LUT) to generate a sinusoidal wave. It may easily extended to generate in-phase and quadrature outputs by adding to the address an offset of $1/4$ of the size of the LUT. By utilizing two-port memory, a compact NCO may be developed. In this radio platform, the NCO was 12 bits wide and the sinusoidal wave represented by 4096 steps.
AM Demodulation

Figure 8: AM demodulation sub system

The AM demodulator utilized an NCO, generating two sinusoidal waves shifted by 90°, as shown in Figure 8. The NCO generated a constant frequency of 100kHz. The outputs of the NCO were 12 bits wide and multiplied with the input from the 12-bit ADC. The outputs of the multiplier were filtered through a bandpass filter with a cutoff of 6kHz and the magnitude of the resulting in-phase and quadrature signals was taken. The signals were truncated to 10 bits before being down-sampled and sent to the DAC.

FM Demodulation

Figure 9: FM demodulation subsystem

The FM demodulator followed a similar pattern, as shown in Figure 9. The phase detector was implemented using a multiplier between the incoming sampled FM signal and the output of the NCO. The transfer function of the loop filter is given by equation:

$$H(z) = \frac{1}{z - 0.0625} \quad (20)$$

The output of the loop filter was passed to the accumulator input of the NCO to generate the appropriate frequency to reduce the phase error to 0. The output for the loop filter contains the demodulated FM signal which was down-sampled to the operating frequency of the DDS and filtered again before being sent to the DAC.
The resources used in the FPGA are show in Table 1. The maximum frequency of operations of the AM demodulator is 150MHz while that of the FM demodulator is 82MHz when individually implemented on the FPGA.

<table>
<thead>
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<th>Memory</th>
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<td>-</td>
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<td>-</td>
<td>16</td>
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<tr>
<td>ADC/DAC Drivers</td>
<td>22</td>
<td>-</td>
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</tr>
</tbody>
</table>

*Table 1: Resources used in the implementation of the units*

**Results and Discussion**

**AM Results**

Before testing the AM demodulator on the FPGA, a number of models were tested on the Modelsim simulator. Figure 10 shows the output of the quadrature direct digital synthesis (DDS). Two waveforms at 90° phase are generated for the IQ demodulator. 8-bit precision was used to generate the waveforms which is a good compromise between accuracy and overall size of the hardware.

*Figure 10: Direct Digital Synthesis (DDS) output waveform*
Figure 11: Demodulation of an AM signal

Figure 11 shows the result of the simulation of demodulating an AM signal. The ‘ADC OUT’ signal shows the AM modulation applied to the system. The ‘DAC IN’ signal shows the demodulated signal. The demodulated signal lags the input signal by several cycles and this is due to delay in the hardware processing.

Finally, the system was tested with a signal from the signal generator. A 200kHz carrier with a 2kHz modulating signal was applied to the system. The amplitude signal was 1V peak. A Tektronix signal generator was used to generate the signal and an Agilent Infiniium MSO8104A oscilloscope was used to visualize the result. Channel 2 shows the AM modulated waveform and Channel 1 shows the original modulating signal. Figure 12 below shows the results. The quality of the output waveform is good but exhibits some negative clipping.

Figure 12: Input and Output waveforms of the AM demodulator

FM Results

Similarly, before the Frequency Modulator (FM) was tested on an FPGA, a series of behavioural models were run to test and optimize its functionality. Figure 13 shows the output of the model of the phase detector, where a sine wave of 22kHz was multiplied by a cosine wave of 24kHz. As one can observe, the high-frequency component is the sum of
the frequencies whilst the low-frequency component is the difference of the frequencies. This would be the signal which would be then fed into the loop filter of the phase locked loop.

**Figure 13:** Output of the phase detector

The whole FM demodulator was tested using a 125kHz carrier signal with a modulating signal of 25kHz. The resulting demodulated signal is a sine wave with a good resolution, as shown in Figure 14.

**Figure 14:** Output of FM demodulation behavioural model

Finally, the FM demodulator was uploaded into the FPGA and tested using a Tektronix Signal generator, using an FM signal modulating a 25kHz baseband signal with a carrier of 125kHz. The results are shown in Figure 15 below. The resulting sine wave signal has a low harmonic distortion.

**Figure 15:** - FM Input and subsequent original demodulated output
Discussion

Both the AM and FM demodulation core worked as intended. The results from the AM demodulator core show more phase delay as the signal takes longer to propagate through the system. For both systems, the modulated signal was provided at baseband. In order to be able to demodulate signals from other bands, a mixer is needed to convert the RF spectrum to baseband. The next section describes further improvements and enhancements that can be carried out to provide more functionality.

Further Improvements

The system was a success, with a sound design methodology being followed during all the phases. Each section of the project was analyzed and a set of specifications for the whole system drawn up. The digital capabilities of the system could be further extended by adding support for more complex modulation techniques, such as Stereo FM, FSK, PSK, and QAM. The board has a good input bandwidth of 12MHz, however, this could be extended. An option is to change the anti-alias filter as the selected ADC supports up to 40MHz. This could allow sampling directly from the antenna by adding a low noise amplifier. Furthermore, a mixer could be added to be able to capture signals in any range. For example, it could be used to receive radio stations in FM band between 88MHz to 108MHz. With its current configuration, the design needs an external frequency generator. If another DAC is added together with an external PLL, any frequency could be synthesized.

Conclusion

A software-defined radio system optimized for an academic setting has been designed and implemented. The radio system is made up of an ADC with a sampling rate of 12MSps and a DAC with a 20kHz bandwidth, together with anti-alias and reconstruction filters. An off-the-shelf FPGA development board has been used. The board was used to implement demodulation of amplitude modulated and frequency modulated signals. It has served to foster an interdisciplinary approach between diverse engineering topics of analog and digital circuit design, as well as digital signal processing and telecommunication techniques. Apart from this, the whole system is affordable and used in various units in the undergraduate program. It also allows the possibility of self-study at home. The results obtained are very encouraging and more projects based on this board are being implemented.
References


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